TC5116405BSJ/BST-60
TC5116405BSJ/BST-70

PRELIMINARY

4,194,304 WORD X 4 BIT (EDO) DYNAMIC RAM

Description

The TC5116405BSJ/BST is the Hyper Page Mode (EDO) dynamic RAM organized as 4,194,304 words by 4 bits. The TC5116405BSJ/BST utilizes Toshiba's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed addressed inputs permit the TC5116405BSJ/BST to be packaged in 26/24 pin plastic SOJ (300mil) and 26/24 pin plastic TSOP (300mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with performance logic families such as Schottky TTL.

Features

- 4,194,304 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 440mW MAX. Operating
  - (TC5116405BSJ/BST-60)
  - 385mW MAX. Operating
  - (TC5116405BSJ/BST-70)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/64ms
- Package
  - TC5116405BSJ: SOJ26-P-300C
  - TC5116405BST: TSOP26-P-300D

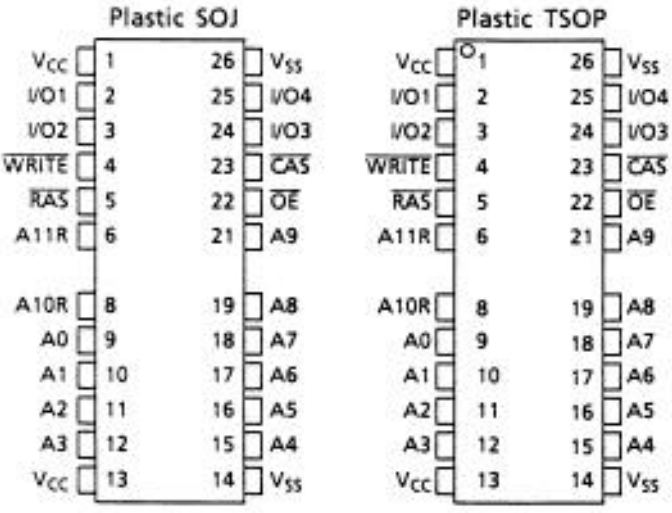
Pin Name

A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

Key Parameters

Item		TC5116405BSJ/BST	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	72ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	17ns	20ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

Pin Connection



TC5117405BSJ/BST-60
TC5117405BSJ/BST-70

PRELIMINARY

4,194,304 WORD X 4 BIT (EDO) DYNAMIC RAM

Description

The TC5117405BSJ/BST is the Hyper Page Mode (EDO) dynamic RAM organized as 4,194,304 words by 4 bits. The TC5117405BSJ/BST utilizes Toshiba's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed addressed inputs permit the TC5117405BSJ/BST to be packaged in 26/24 pin plastic SOJ (300mil) and 26/24 pin plastic TSOP (300mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with performance logic families such as Schottky TTL.

Features

- 4,194,304 word by 4 bit organization
- Fast access time and cycle time
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 605mW MAX. Operating
  - (TC5117405BSJ/BST-60)
  - 523mW MAX. Operating
  - (TC5117405BSJ/BST-70)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 2048 refresh cycles/32ms
- Package
  - TC5117405BSJ: SOJ26-P-300C
  - TC5117405BST: TSOP26-P-300D

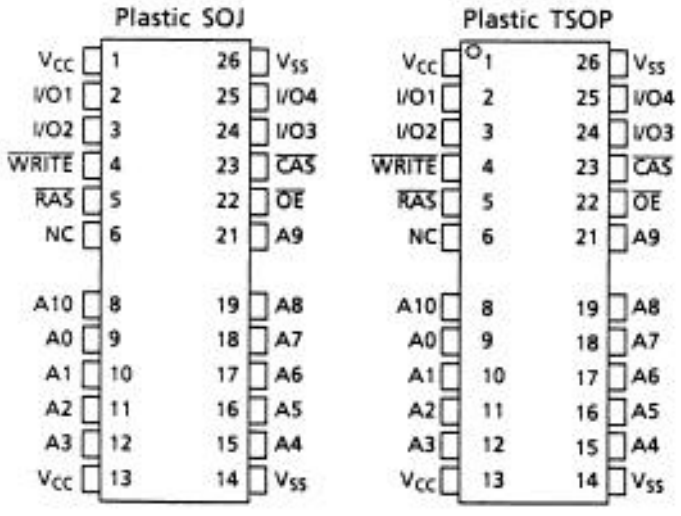
Pin Name

A0~A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Key Parameters

Item		TC5117405BSJ/BST	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	72ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	17ns	20ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

Pin Connection



PRELIMINARY

2,097,152 WORD X 8 BIT (EDO) DYNAMIC RAM

Description

The TC51V17805BNJ/BNT is the Hyper Page Mode (EDO) dynamic RAM organized as 2,097,152 words by 8 bits. The TC51V17805BNJ/BNT utilizes Toshiba's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed addressed inputs permit the TC51V17805BNJ/BNT to be packaged in 28 pin plastic SOJ and 28 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 3.3V±0.3V tolerance, direct interfacing capability with performance logic families such as Schottky LVTTL.

Features

- 2,097,152 word by 8 bit organization
- Fast access time and cycle time
- Single power supply of 3.3V±0.3V with a built-in V_{BB} generator
- Low Power
  - 378mW MAX. Operating
  - (TC51V17805BNJ/BNT-70)
  - 1.8mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- 2048 refresh cycles/32ms
- Package
  - TC51V17805BNJ: SOJ28-P-400C
  - TC51V17805BNT: TSOP28-P-400

Key Parameters

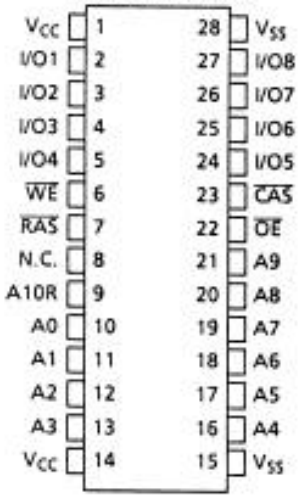
Item		TC51V17805BNJ/BNT
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{AA}	Column Address Access Time	35ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	124ns
t_{HPC}	Hyper Page Mode Cycle Time	30ns

Pin Name

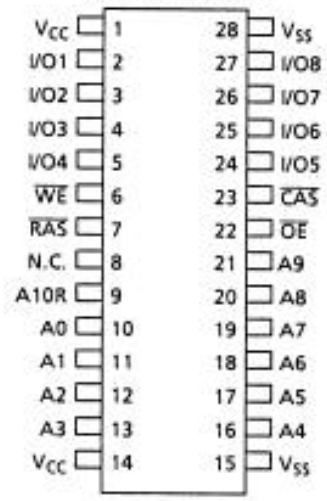
A0~A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O8	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Pin Connection

Plastic SOJ
TC51V17805BNJ



Plastic TSOP
TC51V17805BNT



TC5118165BJ/BFT-60
TC5118165BJ/BFT-70

PRELIMINARY

1,048,576 WORD X 16 BIT (EDO) DYNAMIC RAM

Description

The TC5118165BJ/BFT is the Hyper Page Mode (EDO) dynamic RAM organized as 1,048,576 words by 16 bits. The TC5118165BJ/BFT utilizes Toshiba's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed addressed inputs permit the TC5118165BJ/BFT to be packaged in 42 pin plastic SOJ and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with performance logic families such as Schottky TTL.

Features

- 1,048,576 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 990mW MAX. Operating
  - (TC5118165BJ/BFT-60)
  - 825mW MAX. Operating
  - (TC5118165BJ/BFT-70)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package
  - TC5118165BJ: SOJ42-P-400
  - TC5118165BFT: TSOP50-P-400

Key Parameters

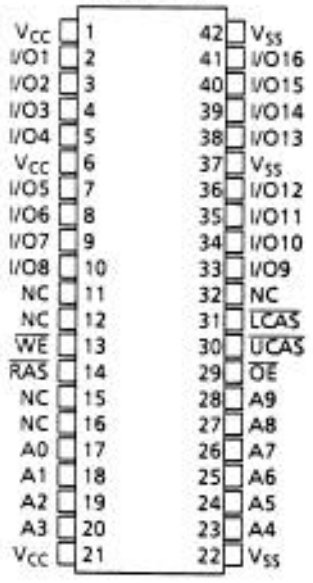
Item		TC5118165BJ/BFT	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	72ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	17ns	20ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

Pin Name

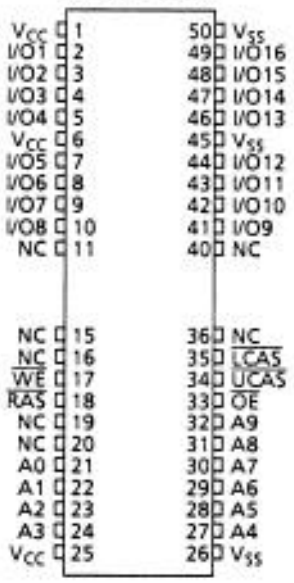
A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Input
$\overline{OE}$	Output Enable
I/O1~I/O16	Data Input/Output
V_{CC}	Power (+5.0V)
V_{SS}	Ground
NC	No Connection

Pin Connection

Plastic SOJ



Plastic TSOP



TC5116165BJ/BFT-60
TC5116165BJ/BFT-70

PRELIMINARY

1,048,576 WORD X 16 BIT (EDO) DYNAMIC RAM

Description

The TC5116165BJ/BFT is the Hyper Page Mode (EDO) dynamic RAM organized as 1,048,576 words by 16 bits. The TC5116165BJ/BFT utilizes Toshiba's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed addressed inputs permit the TC5116165BJ/BFT to be packaged in 42 pin plastic SOJ and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with performance logic families such as Schottky TTL.

Features

- 1,048,576 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 523mW MAX. Operating
  - (TC5116165BJ/BFT-60)
  - 440mW MAX. Operating
  - (TC5116165BJ/BFT-70)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package
  - TC5116165BJ: SOJ42-P-400
  - TC5116165BFT: TSOP50-P-400

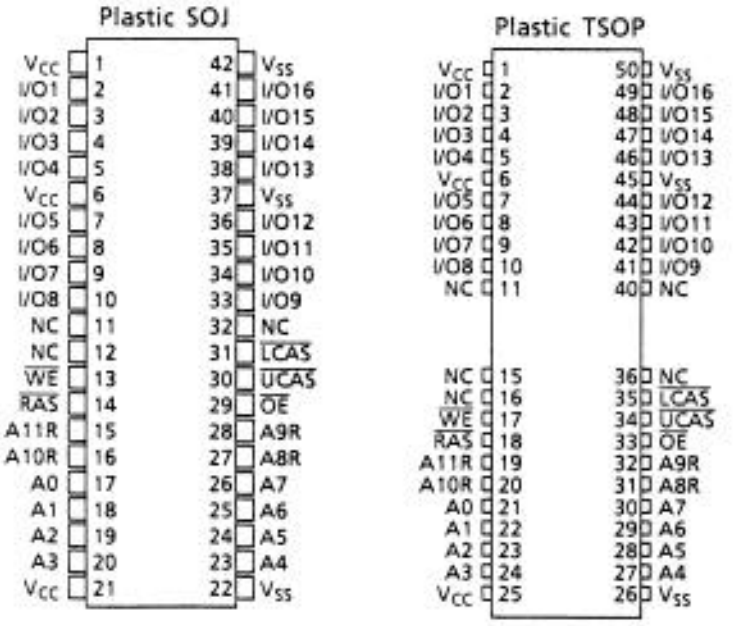
Key Parameters

Item		TC5116165BJ/BFT	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	72ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	17ns	20ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

Pin Name

A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Input
$\overline{OE}$	Output Enable
I/O1~I/O16	Data Input/Output
V_{CC}	Power (+5.0V)
V_{SS}	Ground
NC	No Connection

Pin Connection



PRELIMINARY

1,048,576 WORD X 16 BIT (EDO) DYNAMIC RAM

Description

The TC51V16165BJ/BFT is the Hyper Page Mode (EDO) dynamic RAM organized as 1,048,576 words by 16 bits. The TC51V16165BJ/BFT utilizes Toshiba's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed addressed inputs permit the TC51V16165BJ/BFT to be packaged in 42 pin plastic SOJ and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 3.3V±0.3V tolerance, direct interfacing capability with performance logic families such as Schottky TTL.

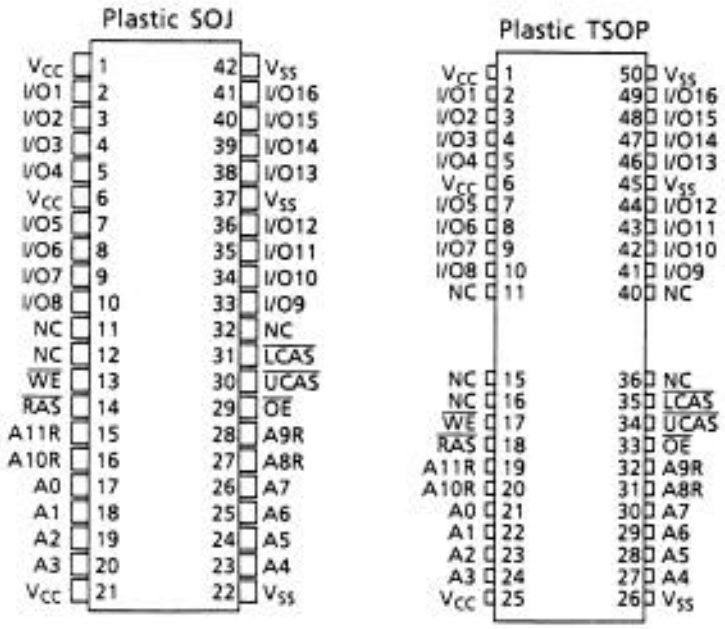
Features

- 1,048,576 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 270mW MAX. Operating
  - (TC51V16165BJ/BFT-60)
  - 1.8mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/64ms
- Package
  - TC51V16165BJ: SOJ42-P-400
  - TC51V16165BFT: TSOP50-P-400

Key Parameters

Item		TC51V16165BJ/BFT
		-70
t_{RAC}	$\overline{RAS}$ Access Time	70ns
t_{AA}	Column Address Access Time	35ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	124ns
t_{HPC}	Hyper Page Mode Cycle Time	30ns

Pin Connection



Pin Name

A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Input
$\overline{OE}$	Output Enable
I/O1~I/O16	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

TC5118325BJ/BFT-60
TC5118325BJ/BFT-70

PRELIMINARY

524,288 WORD X 32 BIT (EDO) DYNAMIC RAM

Description

The TC5118325BJ/BFT is the Hyper Page Mode (EDO) dynamic RAM organized as 524,288 words by 32 bits. The TC5118325BJ/BFT utilizes Toshiba's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed addressed inputs permit the TC5118325BJ/BFT to be packaged in 70 pin plastic SOJ (400mil) and 70 pin plastic TSOP (400mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with performance logic families such as Schottky TTL.

Features

- 524,288 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 1128mW MAX. Operating
  - (TC5118325BJ/BFT-60)
  - 990mW MAX. Operating
  - (TC5118325BJ/BFT-70)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs TTL compatible
- 1024 refresh cycles/16ms
- Package
  - TC5118325BJ: SOJ70-P-400A
  - TC5118325BFT: TSOP70-P-400D

Key Parameters

Item		TC5118325BJ/BFT	
		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	72ns
t_{AA}	Column Address Access Time	30ns	35ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{RC}	Cycle Time	110ns	130ns
t_{HPC}	Hyper Page Mode Cycle Time	25ns	30ns

Pin Name

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS1}$~$\overline{CAS4}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O32	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	NO CONNECTION

TC51V16325BJ/BFT-70
TC51V16325BJ/BFT-80

PRELIMINARY

524,288 WORD X 32 BIT (EDO) DYNAMIC RAM

Description

The TC51V16325BJ/BFT is the Hyper Page Mode (EDO) dynamic RAM organized as 524,288 words by 32 bits. The TC51V16325BJ/BFT utilizes Toshiba's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed addressed inputs permit the TC51V16325BJ/BFT to be packaged in 70 pin plastic SOJ (400mil) and 70 pin plastic TSOP (400mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with performance logic families such as Schottky LVTTL.

Features

- 524,288 word by 32 bit organization
- Fast access time and cycle time
- Single power supply of 3.3V±0.3V with a built-in V_{BB} generator
- Low Power
  - 342mW MAX. Operating
  - (TC51V16325BJ/BFT-70)
  - 306mW MAX. Operating
  - (TC51V16325BJ/BFT-80)
  - 1.8mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Hyper Page Mode (EDO) and Test Mode capability
- All inputs and outputs LVTTL compatible
- 4096 refresh cycles/64ms
- Package
  - TC51V16325BJ: SOJ70-P-400A
  - TC51V16325BFT: TSOP70-P-400D

Key Parameters

Item		TC51V16325BJ/BFT	
		-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns
t_{AA}	Column Address Access Time	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{RC}	Cycle Time	130ns	150ns
t_{HPC}	Hyper Page Mode Cycle Time	30ns	35ns

Pin Name

A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS1}$~$\overline{CAS4}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O32	Data Input/Output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	NO CONNECTION